IBM INDUSTRIAL PRODUCTS

AND INVERTER (AI-2A) MODULE P/N 841551

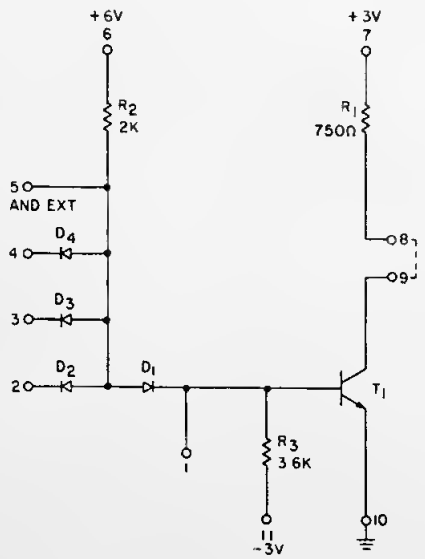
Functional Description

The AND Inverter, AI-2A module consists of three diode positive AND circuits followed by a saturating transistor inverter.

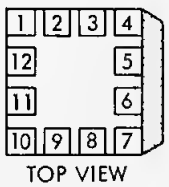
Pins 2, 3 and 4 are the AND inputs, connecting Pin 5 to common anode diodes (FDD module) to extend the AND Fan In.

The OR function can be accomplished by dotting collectors (parallel connected collectors) with other modules - only one collector resistor is required.

Schematic



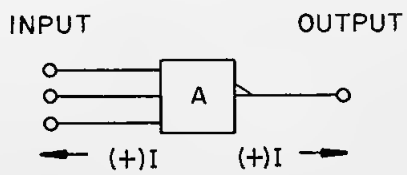
Terminal Configuration



Mechanical Chamfer Right Side

Pins 1 and 12 Leave Open

Block Diagram



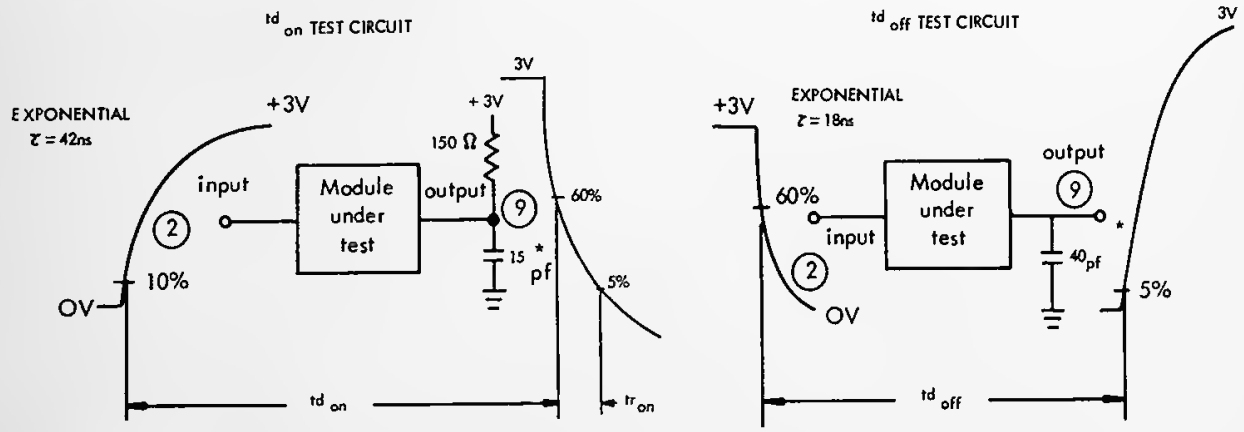
Maximum Ratings

Input Valtage = 13V
Output Valtage = 8V
I_E = 24 Milliamps

AI-2A Module Functional Tests

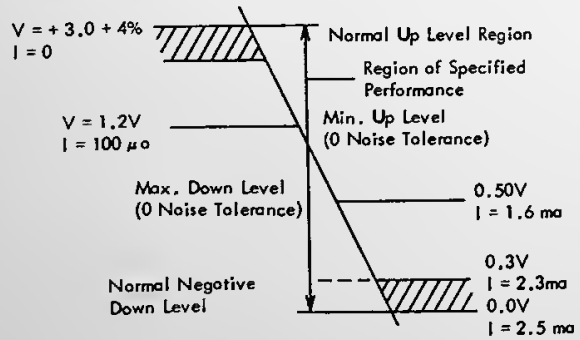
TESTS	TERMINAL CONDITIONS												°C	ADDITIONAL LOAD REQUIREMENTS	VARIABLE	LIMITS		UNITS
	1	2	3	4	5	6	7	8	9	10	11	12				MIN	MAX	
DC ON		+1.2V	+1.2V	+1.2V		+5.76V	+3.12V	V_0	V_0	GND	-3.12V		25/75	18.5 ma CURRENT INTO TERM 8	V_0		0.30	V
DC ON		+1.2V	+1.2V	+1.2V		+5.76V	+3.12V	V_0	V_0	GND	-3.12V		25		V_0		0.17	V
DC OFF		+0.4V	+6.0V	+6.0V		+6.24V	+2.88V	V_0	V_0	GND	-2.88V		25		V_0	2.84		V
DC OFF		+6.0V	+0.4V	+6.0V		+6.24V	+2.88V	V_0	V_0	GND	-2.88V		25		V_0	2.84		V
DC OFF		+6.0V	+6.0V	+0.4V		+6.24V	+2.88V	V_0	V_0	GND	-2.88V		25		V_0	2.84		V
DC NOISE					+1.07V		+2.88V	V_0	V_0	GND	-2.88V		75		V_0	1.8		V
td_{on}		INPUT	+3V	+3V		+6V	+3V	15 pf CAP TO GND	OUTPUT	GND	-3V		25	150Ω RESISTOR TIED BETWEEN TERM 7&8	td_{on}	8	25	ns
tr_{on}		INPUT	+3V	+3V		+6V	+3V	15 pf CAP TO GND	OUTPUT	GND	-3V		25	150Ω RESISTOR TIED BETWEEN TERM 7&8	tr_{on}	5	28	ns
td_{off}		INPUT	+3V	+3V		+6V	+3V	40 pf CAP TO GND	OUTPUT	GND	-3V		25/75		td_{off}	11	35/42	ns

Test Waveforms

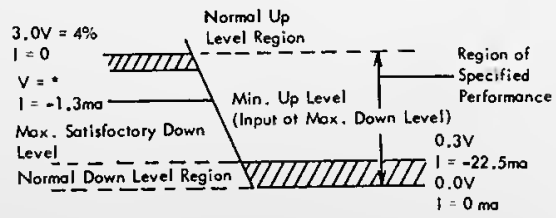


* Including Probe Capacitance

Input Requirements



Output Specifications



* Voltage as defined by collector load impedance

Fan In

Can be extended to a totol of 15 inputs

Fan Out

Totol collector current for the AOI-2A = 22.5ma

$22.5ma \geq I_{R_1} + N_1 K_1 + N_2 K_2 + - - -$

I_{RC} = Total collector lood current

N_1 = Number of AI-2A loads

N_2 = Number of AOI-2A loods

K_1 = 2.3ma, AI - 2A looding constont

K_2 = 3.0ma, AOI - 2A loading constant

To double the Fan Out, the output collectors ond inputs must be paralleled.

Maximum Power Supply Current Requirements

	ON	OFF
+6V	2.5ma	2.8ma
+3V	4.0ma	0
-3V	1.1ma	1.0ma

Maximum Power Dissipation

ON	OFF
35mw	20mw

Average Normal Power Dissipation $= \frac{\text{NOMINAL ON + NOMINAL OFF}}{2} = 25mw$

General Wiring Rules (For Printed Circuit Wire - 10Mil Width Lines)

The input single line length should be less thon 18 inches to prevent excessive reflections ond noise coupling. Maximum length ot either input or output should be less thon 60 inches unless longer deloys specified con be tolerated.